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10/085,773	02/26/2002	Robert Bruce Ganton	UTL 00080	1999

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EXAMINER	
PATEL, HETUL B	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 02/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,773	GANTON, ROBERT BRUCE	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *44-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *44-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communication filed on January 19, 2005. This amendment has been entered and carefully considered. Claims 44-63 are again presented for examination.

2. The objection to drawings (Fig. 7) cited in the previous office action is withdrawn during interview with Attorney on January 03, 2005.

3. Applicant's arguments filed on January 19, 2005 have been fully considered but they are not deemed to be persuasive.

4. Applicant's arguments filed on January 19, 2005 have been fully considered but deemed to be moot in view of new ground rule rejection.

Claim Objections

5. Claims 49 and 50 are objected to because of the following informalities:

It should be stated as "... serially-addressed memory is ..." instead of "... serially-addressed is ..." as disclosed in line 2 of claims 49 and 50.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 44-48, 50-58, 60-61 and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon (USPN: 2003/0050087) in view of Lofgren et al. (USPN: 2002/0032843) hereinafter, Lofgren.

As per claims 44, Kwon teaches a wireless communications device, comprising:

- a non-volatile memory for storing data (NAND-type flash memory 210 in Fig. 2A);
- a processing unit (the combination of 215 and 220 in Fig. 2A) directly connected to the non-volatile memory by parallel address and data lines (222 and 224 in Fig. 2A), the processing unit having: an interface (215 in Fig. 2A) for reading data from the non-volatile memory upon a power on condition, the processing unit outputting at least a portion of the data read from the non-volatile memory onto parallel address (224 thru 215 in Fig. 2A) and data lines (222 in Fig. 2A) to a volatile memory (230 and 235 in Fig. 2A); the volatile memory (230 and 235 in Fig. 2A) connected to the processing unit (the combination of 215 and 220 in Fig. 2A) by the parallel address (224 thru 215 in Fig. 2A) and data lines (222 in Fig. 2A), the volatile memory for storing the at least a portion of the data read from the non-volatile memory for later use by the processing unit (e.g. see paragraph 26, lines 11-18);
- a communications circuit (analog circuit 240 in Fig. 2A) connected to the processing unit, the processing unit controlling the communications circuit

utilizing the at least a portion of the data read from the volatile memory, the communications circuit comprising:

- a transmitter circuit (embedded in 240 of Fig. 2A);
- a receiver circuit (embedded in 240 of Fig. 2A); and
- an antenna (ANT in Fig. 2A) connected to the transmitter circuit and the receiver circuit (e.g. see paragraphs 24-26 on page 2).

Kwon teaches the claimed invention as described above but failed to teach that the non-volatile memory is a serially-addressed memory accessible by a serial address and data line and the processing unit has a serial memory interface.

However, it is well-known and notorious old in the art that the use of a serially-addressed memory accessible by a serial address and data line instead of a parallel-addressed memory accessible by a parallel address and data line is advantageous. Compared to the parallel-addressed memory, the serially-addressed memory: (i) is cheaper so a large size of it can be used with a very little cost; (ii) using a less pin-count and (iii) has a straight forward and low cost structure. The Examiner herein taking Official Notice on this subject matter.

Lofgren teaches the further limitation of having a serial interface. Lofgren teaches that by having a serial interface, a controller can be designed to support memory devices of differing capacities without modifications to the system (e.g. see page 4, paragraph 60). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the serial interface controller as taught by Lofgren in Kwon's device. In doing so, future memory devices of

different capacities can be connected to the same controller without hardware changes resulting in forward and backward compatibility between different memory modules. Also, it is well-known and notorious old in the art that by using a serial interface instead of parallel interface, less hardware (i.e. pin counts) is required. Therefore, it is being advantageous.

As per claims 56, Kwon teaches a method for managing a wireless communications device, comprising the steps of:

- executing instructions from a read-only memory (ROM of ASIC 215 in Fig. 2A) in a processing unit (the combination of 215 and 220 in Fig. 2A), which is directly connected to a non-volatile memory (the NAND-type flash memory 210 in Fig. 2A); and
- transferring the parallel data (i.e. data and address in parallel) to a volatile memory (RAM1 and RAM2, 230 and 235 in Fig. 2A) over parallel address and data lines (222 and 224 in Fig. 2A).

Furthermore, Kwon discloses that the program stored in the non-volatile memory (the NAND-type flash memory) gets copied into the volatile addressable memory (the RAM1) to execute that program by the RAM2 (e.g. see paragraph 25 on page 2). The volatile memory (RAM1 and RAM2) of the wireless communications device (the mobile phone) taught by Kwon is smaller in size compare to the non-volatile memory (the NAND-type flash memory). Therefore, when the interface controller (the MPU) requests the data stored in the indirectly-read memory, the device has to transfer only a portion of the data stored in the non-volatile memory to the addressable volatile memory due to

the limited space and if the interface controller requests the another data, which is currently not stored in the addressable volatile memory, the memory interface will transfer that data to the addressable volatile memory for further processing, i.e. the operation of the communications circuit of the wireless communications device in response to the at least a portion of the transferred data gets started.

The further limitation of using a serially-addressed memory accessible by a serial address and data line instead of a parallel-addressed memory accessible by a parallel address and data line is well-known and notorious old in the art. Compared to the parallel-addressed memory, the serially-addressed memory: (i) is cheaper so a large size of it can be used with a very little cost; (ii) using a less pin-count and (iii) has a straight forward and low cost structure. The Examiner herein taking Official Notice on this subject matter.

The further limitation of converting the serial data to parallel data is well-known and notorious old in the art. The common knowledge or well-known in the art statement is taken to be admitted prior art because applicant presents no arguments to traverse the examiner's assertion of official notice (see MPEP 2144.03 (C)).

Although, Kwon teaches the method comprising a parallel interface controller (215 in Fig. 2A) to read the parallel data from the non-volatile memory (e.g. see Fig. 2A), Kwon does not teach that the method comprises a serial interface controller to read the serial data from the non-volatile memory over a serial address and data line. Lofgren, on the other hand, teaches that by having a serial interface, a controller can be designed to support memory devices of differing capacities without modifications to the system (e.g.

see page 4, paragraph 60). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the serial interface controller as taught by Lofgren in Kwon's device. In doing so, future memory devices of different capacities can be connected to the same controller without hardware changes resulting in forward and backward compatibility between different memory modules. Also, it is well-known and notorious old in the art that by using a serial interface instead of parallel interface, less hardware (i.e. pin counts) is required. Therefore, it is being advantageous.

As per claims 61, Kwon teaches a wireless communications device, comprising:

- a wireless communications circuit (analog circuit 240 in Fig. 2A) comprising;
    - o a receiver (embedded in 240 of Fig. 2A);
    - o a transmitter (embedded in 240 of Fig. 2A); and
    - o an antenna (ANT in Fig. 2A) connected to the receiver and the transmitter;
- a serial non-volatile memory (NAND-type flash memory, 210 in Fig. 2A, which is referred as serial flash memory in the 'Background of the Invention' section of this application);
- a volatile memory (first and second RAM 230, 235 in Fig. 2A); and
- a processor (the combination of 215 and 220 in Fig. 2A) connected to the wireless communications circuit, the processor comprising:
    - o a read only memory (ROM of ASIC 215 in Fig. 2A) for storing read instructions;

- a serial interface connected to the volatile memory (RAM1 and RAM2, 230 and 235 in Fig. 2A) by parallel address and data lines (222 and 224 in Fig. 2A); and
- wherein the processor controls the wireless communications circuit based upon the stored parallel data in the volatile memory (e.g. see paragraph 31 on page 3).

The further limitation of using a serially-addressed memory accessible by a serial address and data line instead of a parallel-addressed memory accessible by a parallel address and data line is well-known and notorious old in the art. Compared to the parallel-addressed memory, the serially-addressed memory: (i) is cheaper so a large size of it can be used with a very little cost; (ii) using a less pin-count and (iii) has a straight forward and low cost structure. The Examiner herein taking Official Notice on this subject matter.

However, Kwon does not teach that the processing unit comprises the ROM, i.e. ROM is a part of the processing unit. However, it is very well known in the art that by fabricating the multiple components on the same chip can reduce the data latency and therefore increases the overall performance of the system. The common knowledge or well-known in the art statement is taken to be admitted prior art because applicant presents no arguments to traverse the examiner's assertion of official notice (see MPEP 2144.03 (C)).

The further limitation of converting the serial data to parallel data is well-known and notorious old in the art. The common knowledge or well-known in the art statement is

taken to be admitted prior art because applicant presents no arguments to traverse the examiner's assertion of official notice (see MPEP 2144.03 (C)).

Although, Kwon teaches the method comprising a parallel interface controller (215 in Fig. 2A) to read the parallel data from the non-volatile memory during boot-up (e.g. see Fig. 2A), Kwon does not teach that the method comprises a serial interface controller, which is directly connected to the non-volatile memory, to read the serial data from the non-volatile memory over a serial address and data line during boot up condition. Lofgren, on the other hand, teaches that by having a serial interface, a controller can be designed to support memory devices of differing capacities without modifications to the system (e.g. see page 4, paragraph 60). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the serial interface controller as taught by Lofgren in Kwon's device. In doing so, future memory devices of different capacities can be connected to the same controller without hardware changes resulting in forward and backward compatibility between different memory modules. Also, it is well-known and notorious old in the art that by using a serial interface instead of parallel interface, less hardware (i.e. pin counts) is required. Therefore, it is being advantageous.

As per claims 45-47, 57-58 and 63, the combination of Kwon and Lofgren discloses the claimed invention as described above, and furthermore, Kwon teaches the wireless communications device, wherein the flash (non-volatile) memory can be a NAND-type flash memory (which is referred as serial flash memory in the 'Background of the Invention' section of this application) or a NOR-type flash memory (which is

referred as parallel flash memory in the 'Background of the Invention' section of this application) (e.g. see paragraph 26 on page 2). Accordingly, either the clocked parallel flash memory or the clocked serial flash memory can be used as the non-volatile memory; based on this rationale, claims 45-47, 57-58 and 63 are rejected.

As per claim 48, the combination of Kwon and Lofgren teaches the wireless communications device, which uses the NAND-type flash memory. The NAND-type flash memory is one of the non-volatile memory type being implemented in Kwon's system; in addition, neither Applicant's specification nor the claimed invention disclose that different type of non-volatile memories would yield different function of the system operation. Therefore, any type of non-volatile memories including the indexed addressable memory and the addressable, serially interfaced memory can be used in the place of NAND-type flash memory.

As per claims 50-51 and 60, the combination of Kwon and Lofgren discloses the claimed invention as described above, and furthermore, Kwon teaches the wireless communications device, wherein the addressable volatile memory (RAM1 and RAM2 230, 235 in Fig. 2A) is a Random Access Memory (RAM) (e.g. see lines 8-9 of paragraph 25); in addition, neither Applicant's specification nor the claimed invention disclose that different type of volatile memories would yield different function of the system operation. Therefore, any type of volatile memories including the dynamic random access memory (DRAM) and the static random access memory (SRAM), can be used. Kwon also teaches that the wireless communications device uses the NAND-type flash memory. The NAND-type flash memory (which is referred as indirectly-read

memory in the 'Background of the Invention' section of this application) is one of the non-volatile memory being implemented in Kwon's system; in addition, neither Applicant's specification nor the claimed invention disclose that different type of non-volatile memories would yield different function of the system operation. Therefore, any type of non-volatile memories including Multimedia Card, Smart Media Card, SD Card, and Memory Stick, can be used in place of the NAND-type flash memory.

As per claim 52, the combination of Kwon and Lofgren discloses the claimed invention as described above, and furthermore, Kwon teaches that the power on condition triggers the processing unit to determine whether the serially-addressed memory is connected to the processing unit (i.e. connection of the flash memory is checked by checking the contents of the flash memory in the step 304 of the flow diagram shown in the Fig. 3), and to instruct the serial memory interface to transfer at least a portion of the data from the serially-addressed memory to the volatile memory. Furthermore, Kwon discloses that the program stored in the non-volatile memory (the NAND-type flash memory) gets copied into the volatile addressable memory (the RAM1) to execute that program by the RAM2 (e.g. see paragraph 25 on page 2). The volatile memory (RAM1 and RAM2) of the wireless communications device (the mobile phone) taught by Kwon is smaller in size compare to the non-volatile memory (the NAND-type flash memory). Therefore, when the interface controller (the MPU) requests the data stored in the indirectly-read memory, the device has to transfer only a portion of the data stored in the non-volatile memory to the addressable volatile memory due to the limited space and if the interface controller requests the another data, which is

currently not stored in the addressable volatile memory, the memory interface will transfer that data to the addressable volatile memory for further processing.

As per claims 53-55, the combination of Kwon and Lofgren discloses the claimed invention as described above, and furthermore, Kwon teaches the wireless communications device comprising the NAND-type flash memory which stores all application programs as well as other types of user data (e.g. see lines 3-7 of paragraph 25). Some of these application programs, for example, an operating system and calibration parameters, are critical to the operation of the wireless communications device; and some of these application programs, for example, interface information, a recent call list, display settings, roaming preferences, ringer preferences and a phone book, are not critical to the operation of the wireless communications device. Based on this rationale, claims 53-55 are rejected.

7. Claims 49, 59 and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon in view of Lofgren, further in view of Christensen et al. (EP 1 189 465 A1), hereinafter, Christensen.

As per claims 49, 59 and 62, the combination of Kwon and Lofgren discloses the claimed invention as described above having the serially-addressed non-volatile memory is connected to the processing unit by the serially address and data line. However, both Kwon and Lofgren failed to teach that the serially-addressed memory is removably connected to the processing unit. Christensen, on the other hand, teaches the memory module (5 in Fig. 1) is removably connected to the terminal control means

(2 in Fig. 1) by an interface (4 in Fig. 1) having several connections for exchanging information between the terminal control means and the memory control means (6 in Fig. 1) (e.g. see the abstract and Fig. 1). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to modify the method and device taught by the combination of Kwon and Lofgren by removably connecting the serially-addressed non-volatile memory to the processing unit as taught by Christensen. In doing so, the removable memory advantageously combines an extended memory function and a subscriber identity module function. Therefore, it is being advantageous.

Remarks

8. As to the remark, Applicant asserted that

(a) Kwon does not teach or disclose a serially addressed memory that is directly connected to the processing unit via a serial address and data line.

(b) Lofgren is also deficient in this area and teaches only a parallel bus architecture connecting the processing unit to the mass storage memory device.

(c) Because of the dominant use and specific advantages of using parallel memory in a cell phone device, one having skilled in the art would not be motivated to connect a serial memory to a processor by a serial address and data line.

Examiner respectfully traverses Applicant's remark for the following reasons:

With respect to (a) and (b), Kwon teaches that the parallel-addressed memory (the NAND-type flash memory 210 in Fig. 2A) is directly connected to the processing unit (the combination of 215 and 220 in Fig. 2A) via a parallel address and data line (222 and 224 in Fig. 2A). It is well-known and notorious old in the art that the use of a serially-addressed memory accessible by a serial address and data line instead of a parallel-addressed memory accessible by a parallel address and data line is advantageous. Compared to the parallel-addressed memory, the serially-addressed memory: (i) is cheaper so a large size of it can be used with a very little cost; (ii) using a less pin-count and (iii) has a straight forward and low cost structure.

With respect to (c), Examiner traverses Applicant's argument about one having skilled in the art would not be motivated to connect a serial memory to a processor by a serial address and data line because compare to the parallel-addressed memory, the serially-addressed memory: (i) is cheaper so a large size of it can be used with a very little cost; (ii) using a less pin-count and (iii) has a straight forward and low cost structure. Therefore, one having skilled in the art WOULD BE motivated to connect a serial memory to a processor by a serial address and data line.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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